Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A dynamic repeater comprising:

an input gate including an input transistor having an input node and two or more clocked input gates operative to place the repeater in a pre-charge mode in response to a first clock signal and to place the repeater in an evaluate mode in response to a second clock signal; ~~and~~

an output node ~~operative to output a voltage of Vcc/2 in response to a voltage of Vcc/2 on the input node in the evaluate mode~~; and

a plurality of transistors coupled between the input transistor and the output node,

wherein the input transistor and said plurality of transistors are sized in a ratio such that the output node is operative to output a voltage of Vcc/2 in response to a voltage of Vcc/2 on the input node in the evaluate mode.

2. (Original) The repeater of claim 1, wherein the clocked transistors include a PMOS transistor coupled to Vcc and an NMOS transistor coupled to Vss, the input transistor being connected between said PMOS and NMOS transistors.

3. (Currently amended) The repeater of claim 1, further comprising:

an intermediate node coupled to one of a source and a drain of the input transistor;

an output inverter having an output coupled to the output node and an input coupled to the intermediate node, and

wherein said plurality of transistors comprise:

a first transistor having a gate coupled to the input node and one of a source and a drain connected to the intermediate node; and

a second transistor connected in series with the first transistor, said second transistor having one of a source and a drain connected to a voltage supply.

4. (Currently amended) The repeater of claim 3, wherein the ~~output inverter~~ repeater has a noise margin of about Vcc/2.

5. (Original) The repeater of claim 3, further comprising a feedback inverter having an input coupled to the intermediate node and an output coupled to a gate of the second transistor.

6. (Canceled)

7. (Original) The repeater of claim 3, wherein the first and second transistors comprise PMOS transistors, wherein the reference voltage is Vcc, and wherein the input transistor is an NMOS transistor.

8. (Original) The repeater of claim 7, wherein the repeater is operative to latch a LOW signal on the intermediate node during the evaluate mode in response to receiving a HIGH data signal at the input node.

9. (Original) The repeater of claim 3, wherein the first and second transistors comprise NMOS transistors, wherein the

reference voltage is Vss, and wherein the input transistor is an PMOS transistor.

10. (Original) The repeater of claim 9, wherein the repeater is operative to latch a HIGH signal on the intermediate node during the evaluate mode in response to receiving a LOW data signal at the input node.

11. (Currently amended) A dynamic bus comprising:

a plurality of bus lines, each bus line including

a dynamic driver at an input,

a clocked flip flop at an output,

a plurality of inverting stages connected between the driver and the flip flop, and

a dynamic repeater connected between two of said inverting stages, said dynamic repeater having a noise margin of about Vcc/2, the dynamic repeater comprising:

an input gate including an input transistor having an input node and two or more clocked input gates operative to place the repeater in a pre-charge mode in response to a first clock signal and to place the repeater in an evaluate mode in response to a second clock signal;

an output node; and

a plurality of transistors coupled between the input transistor and the output node,

wherein the input transistor and said plurality of transistors are sized in a ratio such that the output node is operative to output a voltage of Vcc/2 in response to a voltage of Vcc/2 on the input node in the evaluate mode.

12. (Original) The bus of claim 11, wherein each bus line includes a first segment and a second segment separated by the dynamic repeater, and

wherein the driver is operative to alternate the first segment between a pre-charge mode and an evaluate mode, and

wherein the dynamic repeater is operative to place the second segment in the evaluate mode while the first segment is in the pre-charge mode and to place the second segment in the pre-charge mode while the first segment is in the evaluate mode.

13. (Original) The bus of claim 12, wherein the dynamic repeater is operative to latch a signal during the evaluate phase regardless of the state of the first segment.

14. (Original) The bus of claim 12, wherein an input node of the driver is operative to be pre-charged to a first signal, and wherein an input node of the repeater is operative to be pre-charged to the first signal.

15. (Original) The bus of claim 14, wherein the driver is operative to switch between the pre-charge mode and the evaluate mode in response to a first clock signal and the repeater is operative to switch between the pre-charge mode and the evaluate mode in response to a second clock signal,

wherein the second signal is approximately the inverse of the first signal.

16. (Original) The bus of claim 12, wherein an input node of the driver is operative to be pre-charged to a first signal, and wherein an input node of the repeater is operative to be pre-charged to a second signal,

wherein the second signal is the inverse of the first signal.

17. (Original) The bus of claim 16, wherein the driver is operative to switch between the pre-charge mode and the evaluate mode in response to a first clock signal and the repeater is operative to switch between the pre-charge mode and the evaluate mode in response to the first clock signal.